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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,036	08/20/2003	Yu-Seock Yang	P-0576	5075

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EXAMINER	
LEADER, WILLIAM T	
ART UNIT	**PAPER NUMBER**
1742	

DATE MAILED: 10/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/644,036	YANG ET AL.	
	Examiner	Art Unit	
	William T. Leader	1742	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2006 and 05 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/20/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Receipt of the papers filed on September 9, 2005, is acknowledged. Claims 1-19 are pending. In view of the Japanese patent cited by applicant in the Information Disclosure Statement filed on July 20, 2006, the rejections and objections of record are withdrawn and the following rejections made.

Claim Rejections - 35 USC § 112

2. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. The expression "the electrolyte layer" lacks antecedent basis. The meaning of the term "electrolyte layer" is not clear for the reasons given in the previous action.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 2-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Japanese patent publication 2001-110939, hereinafter Hirobumi et al. An English language computer translation by the National Center for Industrial Property Information and Training at www.ipdl.ncipi.go.jp/homepg_e.ipdl is provided.

6. The Hirobumi et al publication is directed to a method of manufacturing a printed circuit board for use as a semiconductor package substrate. The steps of the method are illustrated in figures 1-8. The patent discloses that a copper foil double-sided substrate was provided. See paragraph [0007]. A through hole was formed with a drill or laser. See paragraph [0008]. The part of the circuit board shown in figure 1 includes a top surface referred to as the component side, and a bottom surface referred to as a solder side. Copper circuit pattern (2) connected to connection pads is depicted. This corresponds to instant claim 2, lines 2-3. Solder resist (4) is formed on both sides of the substrate and in through hole 3. The solder resist may be a photoresist. See paragraph [0010]. This corresponds to instant claim 2, line 14. The solder resist was subjected to ultraviolet ray exposure and development to form a pattern. See step 1) of the example. As shown in figure 1, the pattern includes an opening for a connection pad in the top surface. The opening exposes part of the underlying circuit pattern (2). The opening on the bottom surface may be considered to be a power connection portion as recited in instant claim 2, line 16. In step 3) of the example, a non-electrolytic copper coat is deposited on the whole surface. See figure 2. The non-electrolytic copper on the lower solder side contacts copper pattern (2) and serves a conducting layer for connecting between a power connection portion and an external power source as recited in instant claim 2, lines 5-7 and 17-18. See step 6), lines 1-2 of the example. A plating resist (6) was formed over the non-electrolytic copper on the lower solder side. See step 4) of the example and figure 3. This corresponds to instant claim 2, lines 8-9. Power is supplied to the connection pad to be electroplated by supplying power from an external power source through the non-electrolytic copper layer and the connection pad region of

the lower surface through a portion of circuit pattern (2) to electrodeposit nickel and gold. See step 6), lines 1-3 and figure 5. This corresponds to instant claim 2, lines 10-11. After disconnecting from the power source, additional steps were performed in which the opening in the solder resist on the lower solder side were treated. See steps 7-9 and figures 6-8. All steps recited in instant claim 2 are disclosed by Hirobumi et al.

7. With respect to claim 3, Hirobumi et al show in figure 1 that the power connection portion is formed by removing a portion of the solder resist from the lower side to expose a portion of copper pattern (2) which is subsequently contacted by the non-electrolytic copper layer as shown in figure 2. With respect to claim 4, the non-electrolytic copper layer may be deposited from a Rochell salt bath, an EDTA bath, etc., which are electroless processes. See paragraph [0013]. With respect to claim 5, Hirobumi et al disclose that the electroless copper layer may have a thickness of 0.3 micrometers. See step 3) of the example. With respect to claim 6, electrolytic plating is performed step 6) of the example to the desired thickness. This step corresponds to the step illustrated in applicant's figure 4H. With respect to claim 7, a plating resist (6) is deposited over the non-conductive copper layer. See figure 3 and step 4) of the example.

Claim Rejections - 35 USC § 103

8. Claims 8-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art combined with Japanese patent publication 2001-110939, hereinafter Hirobumi et al.

9. The admitted prior art is that found in applicant's specification under the heading "Background of the Invention" and shown in figures 1-3. The admitted prior art shows that a conventional printed circuit board includes a plurality of bonding pads 3 and a plurality of ball pads 4. It is known to electroplate gold onto both the bonding pads and the ball pads.

10. Claim 9 differs from the prior art by reciting a second step of using some of the circuit patterns as a first power connection portion, a third step of covering the surface of the substrate with the ball pad with a plating resist, a fourth step of supplying power to the bonding pad through the first power connection to form a gold-plated layer on the bonding pad and a fifth step of removing the connection from the external power source. These steps are disclosed by Hirobumi et al as explained above. Claim 9 additionally recites a second sequence of similar steps (steps six through eight) in which the ball pads are plated.

11. The prior art is indicative of the level of skill of one of ordinary skill in the art. It would have been obvious to have modified the process of the prior art by utilizing the sequence of process steps disclosed by Hirobumi et al and explained above to have electrolytically coated both the bonding pads and the ball pads with gold because this sequence of steps is shown by Hirobumi et al to provide gold coating in desired connection areas. It would have been obvious to have modified the process of Hirobumi et al by repeating the steps utilized to electroplate gold on the bonding pad portions on the upper surface to plate gold onto the ball pad portions on the lower surface because electroplated gold provides a good contact to both ball pads and bonding pads as shown by the admitted prior art. The dependent claims are generally similar to the dependent claims discussed above, and the limitations recited in these claims are disclosed by

Hirobumi et al as explained above. A step of covering any remaining openings as recited in claims 8, 16 and 18 would have been obvious because the possibility of creating an undesirable short circuit to an exposed conductor would have been eliminated.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William T. Leader whose telephone number is 571-272-1245. The examiner can normally be reached on Mondays-Thursdays and alternate Fridays, 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Roy King, can be reached on 571-272-1244. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

William Leader
October 3, 2006

ROY KING
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